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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/628,532	07/31/2000	Riccardo G. Dorbolo	062891.0370	5610

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Baker Botts LLP
2001 Ross Avenue
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EXAMINER

MAURO JR, THOMAS J

ART UNIT	PAPER NUMBER
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2143

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/628,532

Applicant(s)

DORBOLO, RICCARDO G.

Examiner

Thomas J. Mauro Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2,3,5.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the amendment (Paper # 6) filed on 12/30/2003. Claims 13-30 remain pending. Claims 1-12 have been cancelled. New claims 31-38 have been added.
2. Claims 13-38 are presented for further examination.
3. In response to filed amendment, Examiner has withdrawn the 112 2nd paragraph and claim objection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
5. Claim 13-15, 19-22, 28-33 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024) in view of Gerstel et al. (U.S. 6,256,293) and Galles et al. (U.S. 5,721,819).

Regarding claim 13, Ghai teaches the invention substantially as claimed, a method for associating routing parameters for a switch with line cards serviced by the switch comprising: programming a redirection memory to associate a routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of routing

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parameters to be provided to the switch to service the first line card [**Ghai -- Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. first line card**].

Ghai fails to teach reprogramming the redirection memory to associate the routing parameter set in the routing memory with the second line card in response to an event initiating activation of a second line card in place of the first line card.

Gerstel, however, teaches an event initiating activation of a second line card in place of the first line card [**Gerstel -- Col. 2 lines 53-54 – Second, i.e. spare, line card is activated upon failure of another line card, i.e. event**].

Furthermore, Galles teaches reprogramming or reconfiguring of a router table in response to a fault occurring in the network [**Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 – Col. 22 lines 1-6**].

Both Gerstel and Galles teach methods for redirecting packets around faults or failures that occur in a routing system.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the reprogramming or reconfiguring of a router table (Galles) in response to an event initiating activation of a second line card (Gerstel), as taught by Galles and Gerstel into the invention of Ghai, in order to provide fault-tolerance in a network to limit down time which is flexible to change or reconfigure routing parameters.

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Regarding claim 14, Ghai-Gerstel-Galles teach the invention substantially as claimed, wherein the event is a failure of the first line card [**Gerstel -- Col. 2 lines 53-61 -- Failed line card, i.e. event, causes activation of a spare card**].

Regarding claim 15, Ghai-Gerstel-Galles teach the invention substantially as claimed, further comprising: programming the redirection memory to associate a second routing parameter set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card [**Ghai -- Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 -- A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. second line card**]; and in response to the event initiating activation of the second line card in place of the first line card [**Gerstel -- Col. 2 lines 53-54 -- Event is a failed line card**], reprogramming the redirection memory to associate the second routing parameter set with the first line card [**Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 -- Col. 22 lines 1-6 -- Routing tables are reprogrammed to associate the various nodes with the new route**].

Regarding claim 19, Ghai-Gerstel-Galles teach the invention substantially as claimed, wherein the redirection memory comprises a programmable table storing associations between line cards serviced by the switch and the routing parameter sets in the routing memory for the switch [**Ghai -- Figure 2, Col. 3 lines 63-67 and Col. 4 lines 1-20 -- In memory is stored a routing table which provides the necessary routing information and instructions to handle incoming data and requests**].

Regarding claim 20, Ghai teaches the invention substantially as claimed, the system comprising: a computer-readable medium; and software stored on the computer-readable medium [Ghai -- Col. 3 lines 45-50 – **In order for the host computer to run the software used to monitor and control the system, the code for the software must be stored on a computer-readable medium. Therefore, the reference implicitly teaches the above computer-readable medium limitation**]. The remaining limitations in the claim are similar to the limitations of claim 13 above. Therefore, claim 20 is rejected under the same rationale.

Regarding claims 21 and 22, these are system claims corresponding to the method claimed in claims 14 and 15. They have similar limitations; therefore, claims 21 and 22 are rejected under the same rationale.

Regarding claim 28-30, these are system claims corresponding to the method claimed in claims 13-15. They have similar limitations; therefore, claims 28-30 are rejected under the same rationale.

Regarding claim 31, Ghai teaches the invention substantially as claimed, the system comprising: logic encoded in media to execute steps [Ghai -- Col. 3 lines 45-50 – **Software used to execute the system is required to have code, i.e. logic, stored on a computer-readable medium**]. The remaining limitations in the claim are similar to the limitations of claim 13 above. Therefore, claim 31 is rejected under the same rationale.

Regarding claim 32-33 and 37, these are logic claims corresponding to the method claimed in claims 14-15 and 19. They have similar limitations; therefore, claims 32-33 and 37 are rejected under the same rationale.

6. Claims 16, 23 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024), Gerstel et al. (U.S. 6,256,293) and Galles et al. (U.S. 5,721,819), as applied to claims 13 and 20 above respectively, in view of Madonna et al. (U.S. 5,598,409).

Regarding claim 16, Ghai-Gerstel-Galles teach the invention substantially as claimed, as aforementioned in claim 13 above, but fail to explicitly teach the routing parameters comprise instructions, instruction sets and an instruction memory.

Madonna, however, teaches, wherein the routing parameters comprise instructions [**Madonna -- Col. 6 lines 10-12 -- Port instructions**], the routing parameter set comprises an instruction set [**Madonna -- Col. 6 lines 10-11 -- Set is just a grouping of instructions, i.e. instructions as to how to control a port**] and the routing memory comprises an instruction memory [**Madonna -- Col. 6 line 12 -- Instructions are stored in memory**].

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include the instructions, instruction sets and instruction memory as taught by Madonna into the invention of Ghai-Gerstel-Galles in order to provide code or instructions to the switch for carrying out the necessary functions.

Regarding claim 23, this is a system claim corresponding to the method claimed in claim 16. It has similar limitations; therefore, claim 23 is rejected under the same rationale.

Regarding claim 34, this is a logic claim corresponding to the method claimed in claim 16. It has similar limitations; therefore, claim 34 is rejected under the same rationale.

7. Claims 17-18, 24-25 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024), Gerstel et al. (U.S. 6,256,293), Galles et al. (U.S. 5,721,819) and Madonna et al. (5,598,409), as applied to claims 16 and 23 above respectively, in view of Bartholomew et al. (U.S. 6,147,988).

Regarding claim 17, Ghai-Gerstel-Galles-Madonna teach the invention substantially as claimed, as aforementioned in claim 16 above, but fails to teach the switch is a synchronous switch.

Bartholomew, however, teaches a synchronous switch for exchanging digital information and a time slot interchanger (TSI) [**Bartholomew -- Col. 6 lines 28-38 and Col. 10 lines 24-27 and lines 30-35**]

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate and use the synchronous switch and time slot interchanger (TSI), as taught by Bartholomew into the invention of Ghai-Gerstel-Galles-Madonna, in order to provide improved efficiency and use of bandwidth through-put within the switch.

Regarding claim 23, this is a system claim corresponding to the method claimed in claim 16. It has similar limitations; therefore, claim 23 is rejected under the same rationale.

Regarding claim 34, this is a logic claim corresponding to the method claimed in claim 16. It has similar limitations; therefore, claim 34 is rejected under the same rationale.

7. Claims 17-18, 24-25 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024), Gerstel et al. (U.S. 6,256,293), Galles et al. (U.S. 5,721,819) and Madonna et al. (5,598,409), as applied to claims 16 and 23 above respectively, in view of Bartholomew et al. (U.S. 6,147,988).

Regarding claim 17, Ghai-Gerstel-Galles-Madonna teach the invention substantially as claimed, as aforementioned in claim 16 above, but fails to teach the switch is a synchronous switch.

Bartholomew, however, teaches a synchronous switch for exchanging digital information and a time slot interchanger (TSI) [**Bartholomew -- Col. 6 lines 28-38 and Col. 10 lines 24-27 and lines 30-35**]

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate and use the synchronous switch and time slot interchanger (TSI), as taught by Bartholomew into the invention of Ghai-Gerstel-Galles-Madonna, in order to provide improved efficiency and use of bandwidth through-put within the switch.

Regarding claim 18, Ghai-Gerstel-Galles-Madonna-Bartholomew teach the invention substantially as claimed, wherein the synchronous switch is a time slot interchanger (TSI) **[Bartholomew -- Col. 6 lines 28-38 and Col. 10 lines 24-27 – Time slot interchanger routes information to and from the interface units].**

Regarding claims 24 and 25, these are system claims corresponding to the method claimed in claims 17 and 18. They have similar limitations; therefore, claims 24 and 25 are rejected under the same rationale.

Regarding claims 35 and 36, these are logic claims corresponding to the method claimed in claims 17 and 18. They have similar limitations; therefore, claims 35 and 36 are rejected under the same rationale.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024), in view of Galles et al. (U.S. 5,721,819), Madonna et al. (5,598,409) and Bartholomew et al. (U.S. 6,147,988).

Regarding claim 26, Ghai teaches the invention substantially as claimed, a redirection memory operable to selectively associate [**Ghai -- Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. first line card**] a disparate one of the plurality of line cards [**Ghai -- Col. 3 lines 57-58**]. Ghai fails to teach a time slot interchanger (TSI) operable to switch traffic between time slots, an instruction memory comprising a plurality of instruction sets comprised of a plurality of instructions and a controller to reprogram the redirection memory to change associations with the line cards.

Bart, however, teaches a time slot interchanger to switch traffic between interface units [**Bartholomew -- Col. 6 lines 28-38 and Col. 10 lines 24-27 – Time slot interchanger routes information to and from the interface units**].

In addition, Madonna teaches an instruction memory [**Madonna -- Col. 6 line 12 – Instructions are stored in memory**] comprising a plurality of instruction sets [**Madonna -- Col. 6 lines 10-11 – Set is just a grouping of instructions, i.e. instructions as to how to control a port**] comprised of a plurality of instructions [**Madonna -- Col. 6 lines 10-12 – Port instructions**].

Furthermore, Galles teaches a controller to reprogram the redirection memory to changes associates of the line cards [**Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 – Col. 22 lines 1-6**].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the time slot interchanger (Bartholomew), instruction memory containing instructions (Madonna) and the reprogramming and reconfiguring of routing table, i.e. memory (Galles), as taught by Bartholomew, Madonna and Galles into the invention of Ghai, in order to:

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provide fault-tolerance in a network to limit down time which is flexible to change or reconfigure routing parameters, provide code or instructions to the switch for carrying out the necessary functions, and improve efficiency and use of bandwidth through-put within the switch

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024), Galles et al. (U.S. 5,721,819), Madonna et al. (5,598,409) and Bartholomew et al. (U.S. 6,147,988), as applied to claim 26 above, in view of Gerstel et al. (U.S. 6,256,293).

Regarding claim 27, Ghai-Galles-Madonna-Bartholomew teach the invention substantially as claimed, as aforementioned in claim 26 above, comprising: the redirection memory programmed to associate a first instruction set with a working line card [**Ghai -- Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. first line card**] and a second instruction set with a protect line card [**Ghai -- Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. second line or protect card**]; and the controller operable to reprogram the redirection memory to associate the first instruction set with the protect line card and the second instruction set with the working line card [**Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 – Col. 22 lines 1-6 – Routing tables are reprogrammed to associate the various nodes with the new route**].

Ghai-Galles-Madonna-Bartholomew, fail to teach the activation of the second line card in place of the first line card in response to failure of the first line card.

Gerstel, however, teaches that the second line card, i.e. spare line card, is activated in response to a line card failing [**Gerstel -- Col. 2 lines 53-54 -- Event is a failed line card**].

Both Gerstel and Galles teach methods for redirecting packets around faults or failures that occur in a routing system.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate activating a second line card in place of a first line card in response to a failed line card, as taught by Gerstel into the invention of Ghai-Galles-Madonna-Bartholomew, in order to provide fault-tolerance in a network to limit down time.

10. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ghai et al. (U.S. 6,389,024) in view of Gerstel et al. (U.S. 6,256,293), Galles et al. (U.S. 5,721,819), Madonna et al. (5,598,409) and Bartholomew et al. (U.S. 6,147,988).

Regarding claim 38, Ghai teaches the invention substantially as claimed, a method comprising:

programming a redirection memory to associate a routing parameter set in a routing memory for a switch with a first line card, the routing parameter set including a plurality of routing parameters to be provided to the switch to service the first line card [**Ghai -- Figure 2,**

Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. first line card];

programming the redirection memory to associate a second routing parameter set in the routing memory with the second line card, the second routing parameter set including a plurality of routing parameters to be provided to the switch to service the second line card [Ghai --

Figure 2, Col. 3 lines 57-67 and Col. 4 lines 1-20 – A routing table, containing routing parameters, is stored within memory which handles service requests for the line cards, i.e. second line card]; and a programmable table storing associations between line cards serviced by the switch and the routing parameter sets in the routing memory for the switch [Ghai -- **Figure 2, Col. 3 lines 63-67 and Col. 4 lines 1-20 – In memory is stored a routing table which provides the necessary routing information and instructions to handle incoming data and requests].**

Ghai fails to teach reprogramming the redirection memory to associate the routing parameter set in the routing memory with the second line card in response to an event initiating activation of a second line card in place of the first line card and reprogramming the redirection memory to associate the second routing parameter set with the first line card.

In addition, Ghai fails to teach the routing parameters comprise instructions, instruction sets and an instruction memory, a synchronous switch and a time slot interchanger (TSI).

Gerstel, however, teaches an event initiating activation of a second line card in place of the first line card [Gerstel -- **Col. 2 lines 53-54 – Second, i.e. spare, line card is activated upon failure of another line card, i.e. event]** and wherein the event is a failure of the first line card [Gerstel - **Col. 2 lines 53-61 – Failed line card, i.e. event, causes activation of a spare card].**

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Furthermore, Galles teaches reprogramming or reconfiguring of a router table in response to a fault occurring in the network [Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 – Col. 22 lines 1-6] and reprogramming the redirection memory to associate the second routing parameter set with the first line card [Galles -- Col. 11 lines 55-65 and Col. 21 lines 64-67 – Col. 22 lines 1-6 – **Routing tables are reprogrammed to associate the various nodes with the new route**]; In addition, Madonna further teaches the routing parameters comprise instructions [Madonna -- Col. 6 lines 10-12 – **Port instructions**], the routing parameter set comprises an instruction set [Madonna -- Col. 6 lines 10-11 – **Set is just a grouping of instructions, i.e. instructions as to how to control a port**] and the routing memory comprises an instruction memory [Madonna -- Col. 6 line 12 – **Instructions are stored in memory**].

Lastly, Bartholomew teaches a synchronous switch and wherein the synchronous switch is a time slot interchanger (TSI) [Bartholomew -- Col. 6 lines 28-38 and Col. 10 lines 24-27 and lines 30-35].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the reprogramming or reconfiguring of a router table (Galles) in response to an event initiating activation of a second line card (Gerstel), the synchronous switch and time slot interchanger (Bartholomew) and an instruction memory containing instructions (Madonna), as taught by Galles, Gerstel, Bartholomew, Madonna into the invention of Ghai, in order to: provide fault-tolerance in a network to limit down time which is flexible to change or reconfigure routing parameters, provide code or instructions to the switch for carrying out the necessary functions, and improve efficiency and use of bandwidth through-put within the switch.

Response to Arguments

11. Applicant's arguments with respect to claims 13, 17-18 and 24-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Mauro Jr. whose telephone number is 703-605-1234. The examiner can normally be reached on M-F 8:00a.m. - 4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on 703-308-5221. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


TJM

March 8, 2004


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